Phase locked oscillators

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1 Introduction

WORK Microwave offers a wide selection of high-performance frequency sources. This includes fixed-frequency, frequency-agile with phase-locked sources and frequency synthesizers from 125 MHz to 26 GHz. Our frequency source products are used throughout the world, in commercial and military applications. WORK's highly experienced team of engineers, technicians and assembly people bring today's cutting edge technologies to all of our frequency source products.

1.1 Phase-locked oscillators and synthesizers

Low noise phase-locked frequency sources and synthesizers offer system designers a distinct advantage. Because phase-locked sources have well characterized reliable noise and spurious performance, it allows the system designer to only consider their signal path and frequency planning in the system block. WORK uses several configurations in both the oscillator and synthesizer product lines. High performance single loop and more powerful multi-loop designs give our customers a perfect fit for any system requirement. In addition, our products can be easily customized to meet the most demanding system challenges and extreme environmental conditions.

A well-designed phase-locked frequency source is
both an accurate and stable signal source. Its stability and accuracy are directly related to the stability and accuracy of a lower-frequency reference and can take many forms. It can be a fixed-frequency, high-stability crystal oscillator supplied as an integral part of the phase-locked assembly, or it can be an externally-supplied crystal reference. The reference source is sometimes a phase-locked oscillator itself, locked to a low-frequency standard.

WORK synthesizers are compatible with many standard serial or parallel interfaces to program frequency, and can be customized to meet any user protocol. Standard user interfaces can be downloaded from the WORK web site and operate from any windows based PC.

1.2 Source design approaches

WORK uses both analog and digital phase-locked loop designs in fixed and frequency-agile synthesized sources. An analog design multiplies the reference signal up to the output frequency of the microwave oscillator and uses conventional analog phase detectors and sampling mixer circuits for detection at microwave frequencies. A digital phase-locked loop uses fixed or fractional division ratio dividers for the main signal as well as for the reference signal. Digital phase detectors form the final link of the phase-locked loop coupled with active and passive filtering to tailor noise and spurious performance. Our homegrown resources for many of the internal components used include VCOs, sampling phase detectors, digital phase detectors, fractional dividers, delta/sigma or DDS fractional dividers, and frequency multipliers which help us to independently lead the market with product performance and reliability.

1.3 New product development

WORK continually strives to improve product offerings to meet the demand of today's aerospace, military and earth station radio product needs. In addition to improving our current products we will continue to expand our catalog offerings utilizing the best available components which equates to an improvement in performance, increased value, saved power and an overall decrease in the size of our sources.

1.4 Product line description

In addition to our standard products, WORK offers its customers an extensive custom design capability. Requirements for custom designs can usually be met with minor engineering changes, while others might require extensive design work. We offer custom designs up to as high as 26 GHz with the use of our internally designed frequency multipliers. In addition, we continuously design and manufacture frequency sources for our own SATCOM converters and receivers as well as use our unique product expertise to design sophisticated ECM and communications systems.

If in doubt about the suitability of a particular synthesizer requirement, give our design engineers a call. They can help you to properly select a wide range of output frequency bands, the right frequency resolution, coding, and acquisition times as well as environmental conditions.

1.5 phase locked oscillators

WORK phase-locked oscillator products are rugged modular components that can be used in a wide variety of applications. The phase-locked oscillators have found their way into every type of high quality telecommunications, lab testing, satellite up- and downconverters, radar and many other applications that require the high quality and performance that we design into our products.

The phase locked oscillator design begins by defining the performance parameters required. The most significant of these requirements is usually associated with the frequency band and frequency resolution. Next would be performance requirements such as phase noise, spurious, harmonics, reference, operating voltage and power consumption. These are all factors that must be considered before choosing a phaselocked oscillator design. Phase noise requirements and contributions of either an internal or externally supplied reference will usually dominate the choice or type of design required, followed by frequency resolution. If the output frequency maintains integer multiples of the reference frequency, a simple single analog loop can be applied. If the reference noise is not adequate when multiplied to the output or if the output frequency is not an integer multiple of the reference frequency, we would need to either use a single loop digital approach or introduce a multi-loop design.

Single loop analog designs are preferred due to the very low noise floor the analog phase detector can provide. Generally this noise can be below -160 dBc. In most cases this will do very little to degrade a good reference frequency. The output noise will be degraded only by the frequency multiple of the reference to the output.

With the digital phase-locked loop, the reference frequency can be divided or fractionally divided to allow fine resolution of output frequency. The drawback to the digital loop is usually due to a poorer phase detector noise floor which will result in a higher output loop phase noise. The finer resolution will also adversely affect spurious performance. Digital single loop designs usually incorporate narrow loop bandwidths and higher quality VCO performance to offset these limitations.

The multiple loop design will allow us to utilize the best of the very low noise analog circuits along with digital and analog sub-loops to enable very fine frequency resolution and mask the noise contribution of the reference frequency. This mask effect of the reference noise is another strong attribute of the multiple loop design choice. Multiple loop phase-locked oscillators designed by WORK use a proprietary approach that allows extremely fine resolution without large N multiples that reference division will cause.

2 PLO Specifications

Model number	type	Frequency range	outline	description
PLO-CRO-xxxx-EXT	PLO with external reference	125~2500MHz	52.0 x 67.2 x 15.2 mm³	low cost single loop, single frequency
PLO-CRO-xxxx-TCXO	PLO with internal TCXO	125~2500MHz	57.1 x 68.6 x 15.0 mm³	multi loop, single frequency, high performance
PLO-CRO-xxxx-OCXO	PLO with internal OCXO	10.0~26.5GHz	105.4 x 69.0 x 25.7 mm³	multi loop, single frequency, very low spurious and phase noise, ultra high performance
PLO-CRO-xxxx-XO	PLO with internal crystal	1200~9999.9MHz	52.0 x 130.0 x 15.2 mm³	multi loop, single frequency, very low phase noise, high performance

3 PLO-CRO-xxxx-EXT series

Features

- low phase noise design
- > +10dBm output level
- low spurious and harmonics
- high reference frequency suppression, typical –80dBc
- low power consumption <2W
- input reference typical 10MHz
- low timing jitter, typical 90fs (30Hz to 1MHz offset)

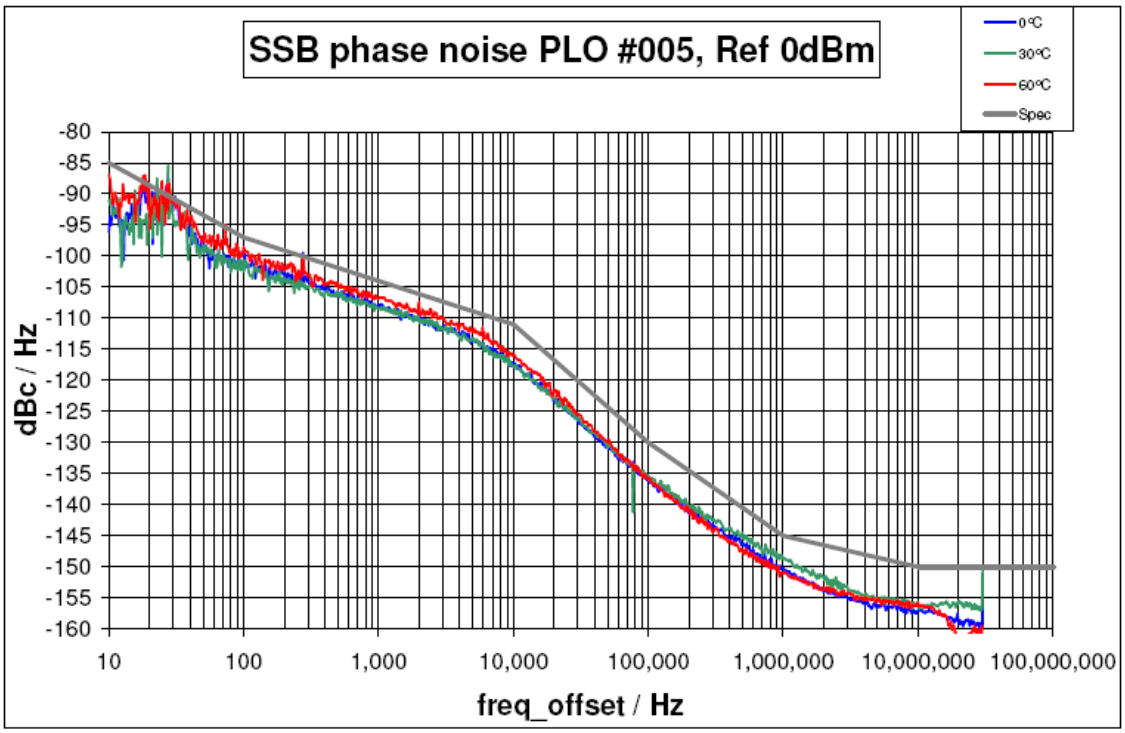
options

- higher output power
- lower power consumption <1.4W

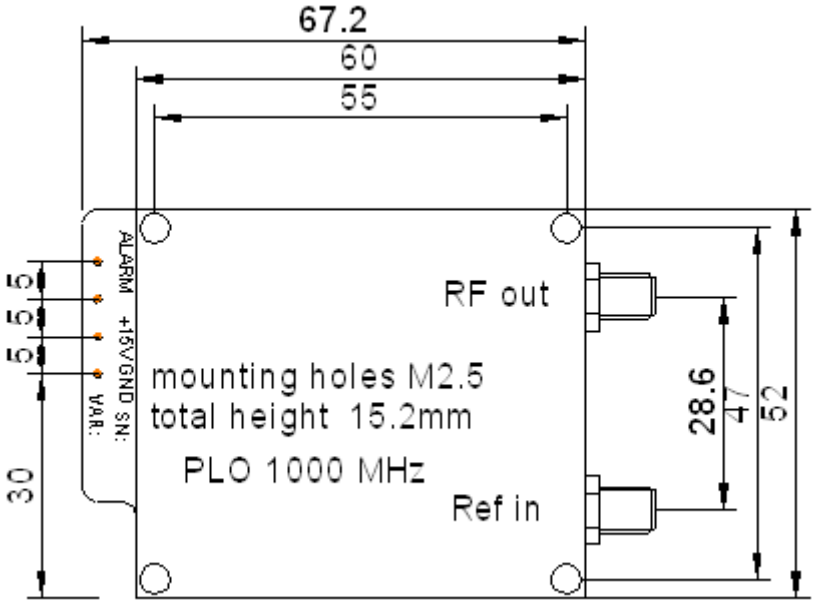
PLO Type:		**PLO-CRO-xxxx-EXT**		
RF-Output Frequency:		125 ... 2500 MHz		
Phase Noise: **(values for 800..1000MHz)**	10 Hz 100 Hz 1 kHz 10 kHz 100 kHz 1 MHz 10 MHz	-85 -97 -104 -111 -130 -145 -150	-87 -98 -106 -115 -132 -147 -155	
		max. values in dBc/Hz	typ. values in dBc/Hz	
Spurious Outputs:		Δf = ±10 MHz: Δf > 10 MHz: Output harmonics:	< -70 dBc < -75 dBc < -50 dBc	
Output level:		 Connector:	>10 dBm SMA (female)	
Timing Jitter:		30Hz … 1MHz offset	< 100fS	
Reference Input:		Frequency: Level: Connector:	10 MHz sine wave 5 dBm ±5 dB SMA (female)	
Lock detect output:		TTL, active high		
Temperature Range:		0 °C … 60 °C operating, -30 °C … 80 °C storage		
Relative Humidity:		< 95 % non condensing		
Power Input:		15V ± 5%		
Power Consumption:		Max: 2 W		
Power and control connector:		Solder point (through hole 1mm)		
Dimension and Weight:		67.2 x 52.0 x 15.2 mm^3 (WxHxD), approx. 75g		

Specifications are subject to change

Typical phasenoise over temperature



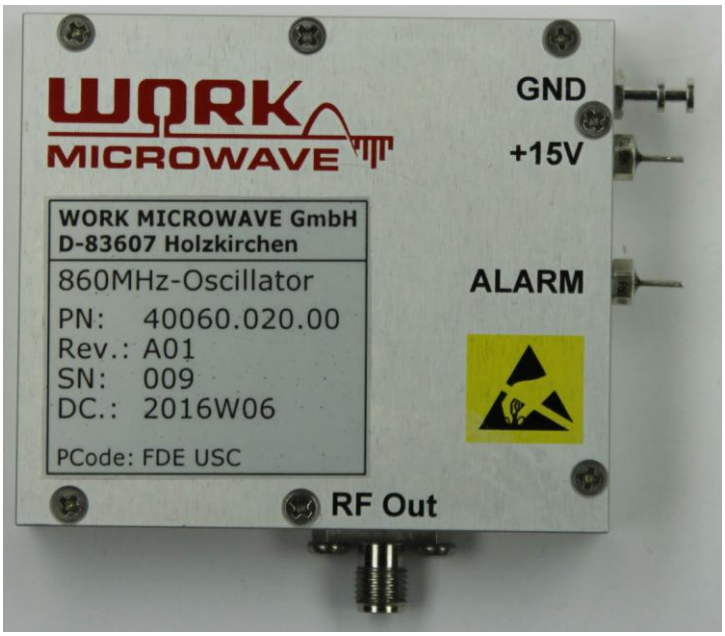
outline dimensions



4 PLO-CRO-xxxx-TCXO series

Features

- very low phase noise design
- high output level, typical +20dBm
- low spurious (typical <-90dBc) and harmonics
- high reference frequency suppression, typical -90dBc
- low power consumption <5W
- frequency stability < 10ppm over temperature and aging over 15 years
- wide operating temperature range -30°C … +70°C



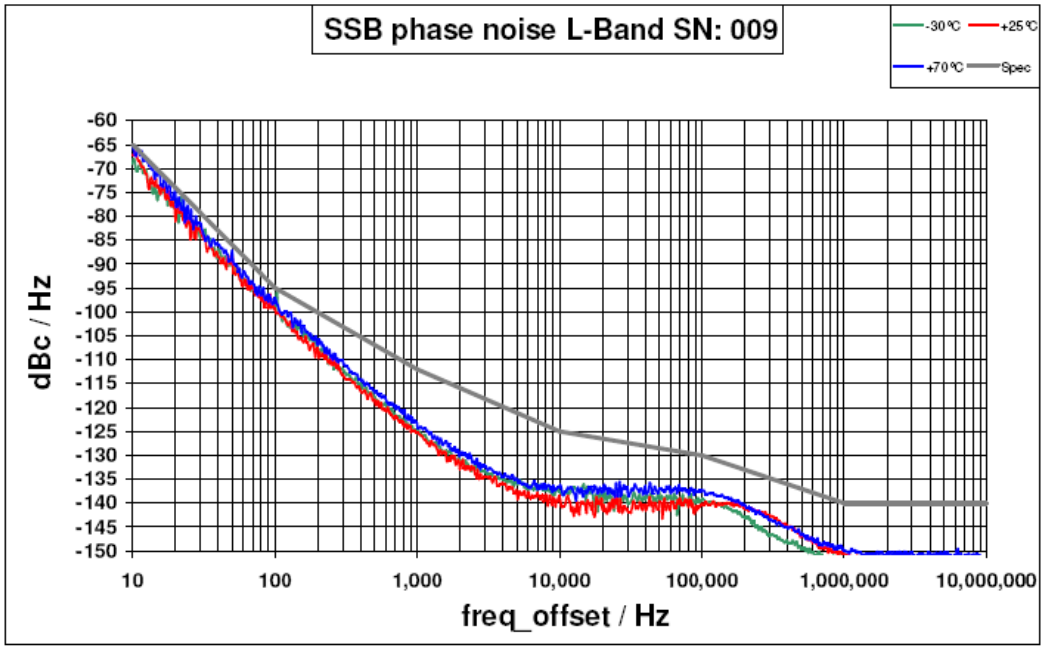
options

- lower power consumption <3.5W with less output level

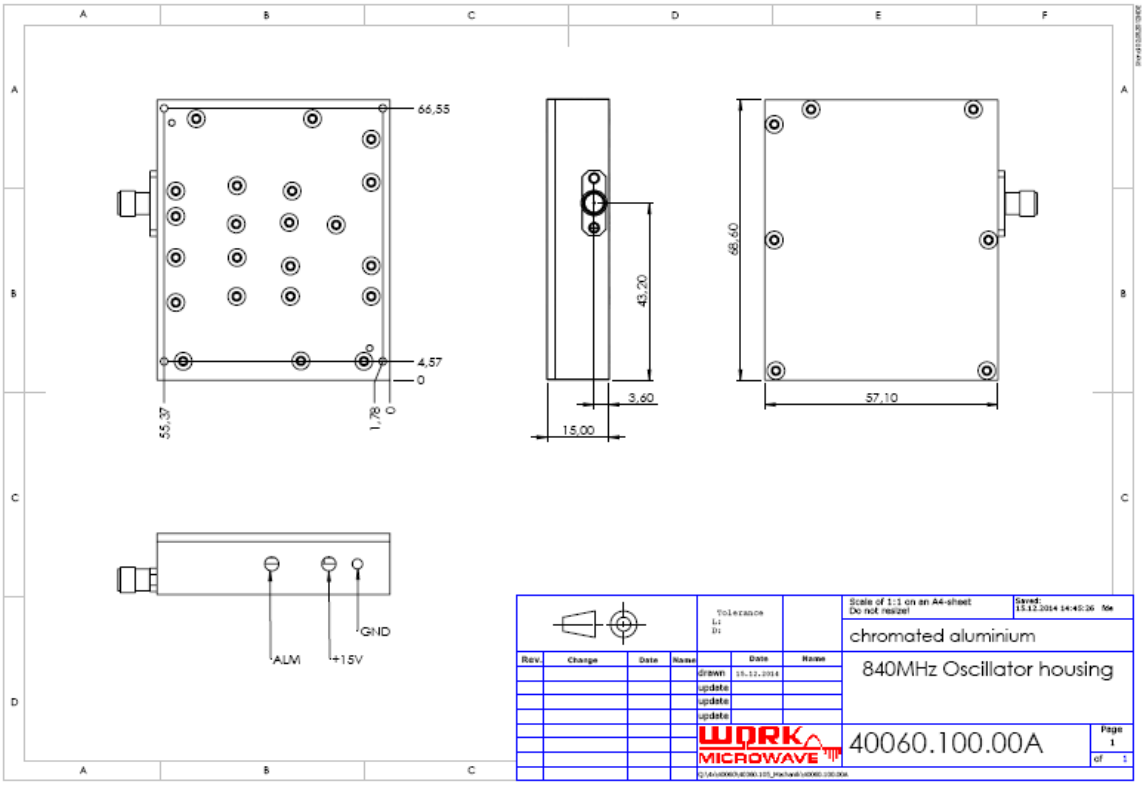
PLO Type:		PLO-CRO-xxxx-TCXO		
RF-Output Frequency:		125 ... 2500 MHz		
Phase Noise: (values for 800..1000MHz)	10 Hz 100 Hz 1 kHz 10 kHz 100 kHz 1 MHz 10 MHz	-65 -95 -112 -125 -130 -140 -150	-66 -97 -123 -136 -137 -150 -152	
		max. values in dBc/Hz	typ. values in dBc/Hz	
Spurious Outputs:		Δf < 20 MHz: Δf > 20 MHz: Output harmonics:	< -80 dBc < -85 dBc < -60 dBc	
Output level:		Connector:	+20 dBm ±2 dB SMA (female)	
Frequency stability:		-20°C … +70°C and aging	< ±10 ppm	
Lock detect output:		TTL, active high		
Temperature Range:		-30 °C … +70 °C operating, -40 °C … 80 °C storage		
Relative Humidity:		< 95 % non condensing		
Power Input:		15V ± 5%		
Power Consumption:		Max: 5 W		
Power and control connector:		Feed-through-capacitor		
Dimension and Weight:		68.6 x 57.1 x 15.0 mm^3 (WxHxD), approx. 120g		

Specifications are subject to change

Typical phasenoise over temperature



outline dimensions



5 PLO-CRO-xx.x-OCXO series

Features

- ultra low phase noise design
- high output level, typical +21dBm
- low spurious (typical <-100dBc) and harmonics
- high reference frequency suppression, typical -100dBc
- frequency stability < 10ppm over temperature and aging over 15 years
- wide operating temperature range -30°C … +70°C

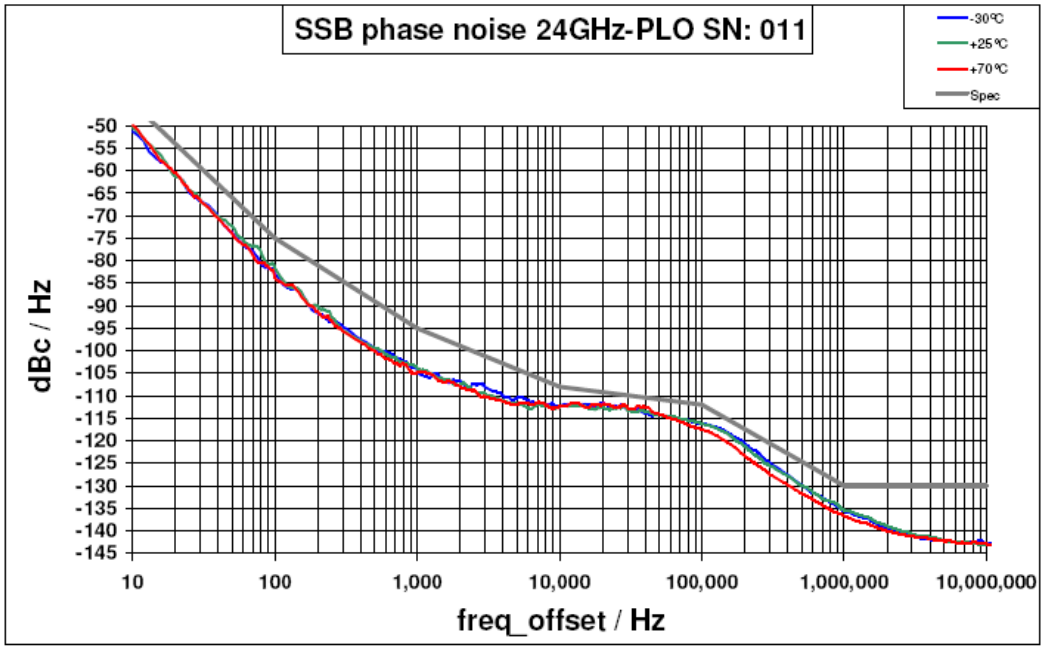
options

- lower power consumption <12W with less output level

PLO Type:		**PLO-CRO-xx.x-OCXO**		
RF-Output Frequency:		10.0 ... 26.5 GHz		
Phase Noise: (values for 800..1000MHz)	10 Hz 100 Hz 1 kHz 10 kHz 100 kHz 1 MHz 10 MHz	-45 -75 -95 -108 -112 -130 -140	-50 -80 -104 -112 -116 -135 -142	
		max. values in dBc/Hz	typ. values in dBc/Hz	
Spurious Outputs:		Δf < 20 MHz: Δf > 20 MHz: Output harmonics:	< -90 dBc < -90 dBc < -60 dBc	
Output level:		Connector:	+21 dBm ±2 dB K (female)	
Frequency stability:		-20°C … +70°C and aging	< ±10 ppm	
Lock detect output:		Alarm contact, active open		
Temperature Range:		-30 °C … +70 °C operating, -40 °C … 80 °C storage		
Relative Humidity:		< 95 % non condensing		
Power Input:		±15V ± 5%, <950mA @ +15V (steady state), <1300mA @ +15V (warm-up), <50mA @ -15V		
Power Consumption:		Max: 15 W steady state, <20W warm-up		
Power and control connector:		Feed-through-capacitor		
Dimension and Weight:		105.4 x 69.0 x 31.2 mm^3 (WxHxD), approx. 325g		

Specifications are subject to change

Typical phasenoise over temperature



PhaseNoise Chart 4

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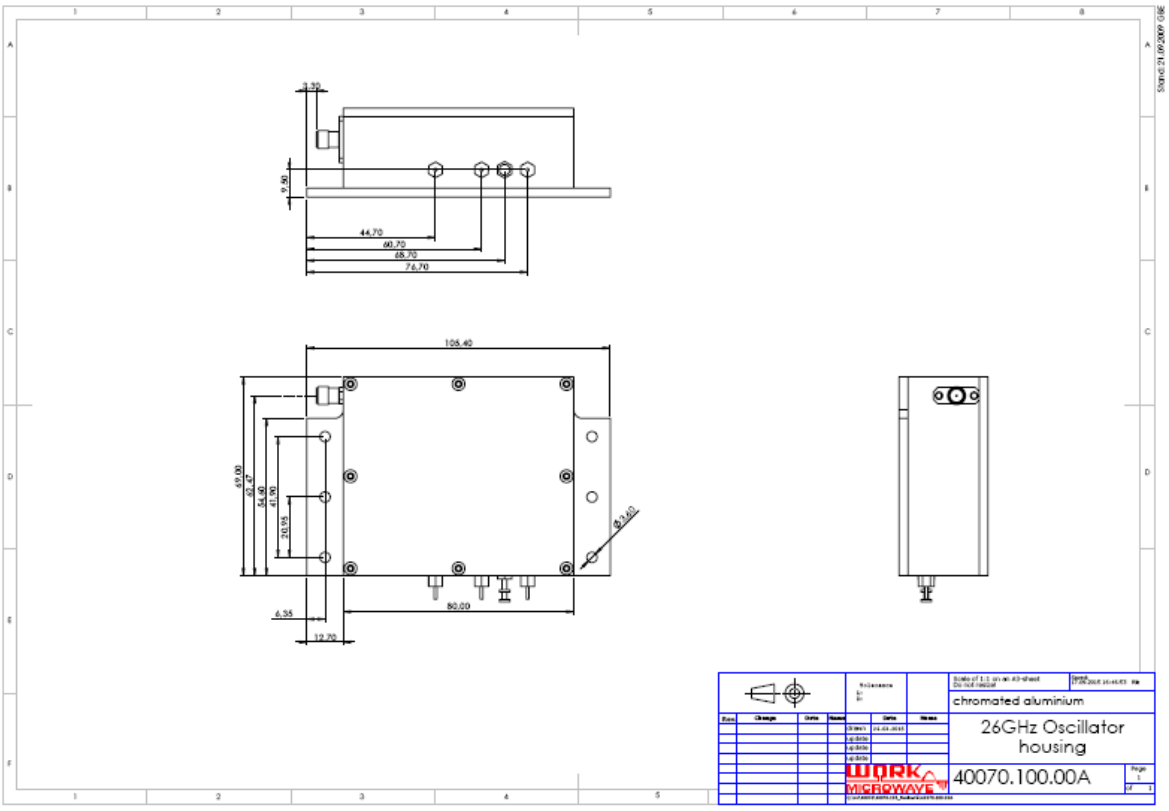
outline dimensions



6 PLO-CRO-xxxx.x-XO series

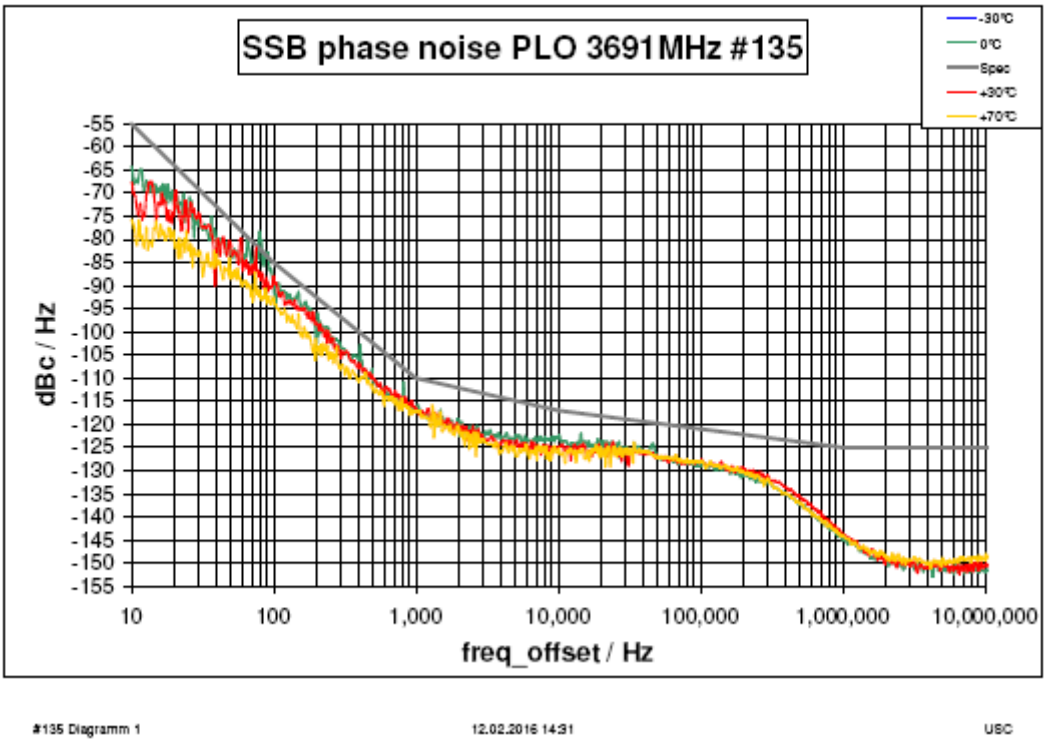
Features

- low phase noise design
- medium output level, typical +10dBm
- low spurious and harmonics
- low power consumption <3W
- frequency stability < 100ppm over temperature and aging over 15 years
- wide operating temperature range -30°C … +70°C

PLO Type:		**PLO-CRO-xxxx.x-XO**		
RF-Output Frequency:		1200.0 ... 9999.9 GHz		
Phase Noise: **(values for 3691MHz)**	10 Hz 100 Hz 1 kHz 10 kHz 100 kHz 1 MHz 10 MHz	-55 -85 -110 -117 -121 -125 -125	-60 -90 -115 -124 -127 -144 -148	
		max. values in dBc/Hz	typ. values in dBc/Hz	
Spurious Outputs:		Δf < 10 MHz: Δf > 10 MHz: Output harmonics:	< -60 dBc < -70 dBc < -50 dBc	
Output level:		Connector:	+10 dBm ±2 dB SMA (female)	
Frequency stability:		-20°C … +70°C and aging	< ±100 ppm	
Lock detect output:		TTL, active high		
Temperature Range:		-30 °C … +70 °C operating, -40 °C … 80 °C storage		
Relative Humidity:		< 95 % non condensing		
Power Input:		7V ± 5%, <430mA		
Power Consumption:		max: 3 W		
Power and control connector:		14-Pin-header, male		
Dimension and Weight:		130.2 x 52.1 x 15.2 mm^3 (WxHxD), approx. 135g		

Specifications are subject to change

Typical phasenoise over temperature



outline dimensions